

Sony's technology highlights

"Exmor" High-Speed CMOS Sensor

Sony developed CMOS Sensor "Exmor", which adopts the "Column-Parallel A/D Conversion Technique" to create images containing more detail than ever before. It combines the speed of the CMOS sensor with advanced-quality image sensor technologies accumulated through the development of CCDs. The result is enhanced resolution along both the space and time axes. With these innovations, Sony is exploring the limitless potential of the world of imaging.

A high-speed imaging sensor must combine high-sensitivity with low noise. In a CMOS sensor, the pixels, signal readout circuit, analog-to-digital conversion circuit and controller are all built into a single chip. By optimizing the composition and operation of each circuit, Sony has achieved previously incompatible goals of increasing both speed and image quality.

Pixel Design Optimized for High Sensitivity	
Reducing Noise	
Row-Column-Row A/D Conversion for Enhanced Speed	
Future Challenges	
Awards	

Pixel Design Optimized for High Sensitivity

When visible light strikes an image sensor, electrons are generated by a photoelectric effect occurring in the silicon from which the sensor is made. Sensitivity is increased by capturing light without waste and efficiently converting it into electrons. Pixels in an image sensor must incorporate a photodiode and provide a number of functions, including signal accumulation start, signal accumulation end, readout pixel selection, and selected pixel signal readout. Each pixel consists of a photodiode and transistors to perform the various tasks. Sensitivity can be enhanced by modifying the transistor array and layout, and by making the photodiode as large as possible. Sony's first priority when it began to develop CMOS sensors was to improve the pixels.

In addition to using a larger photodiode, enhancing sensitivity also requires a system to guide the

light accurately to the photodiode. Figure 1 is a cross-sectional photograph of a pixel. From top to bottom, each pixel consists of a on-chip micro-lens, on-chip color filter, inner lens, wiring, and photodiode. The on-chip micro-lens and inner lens guide the light precisely onto a single pixel measuring less than 2µm across, while the color filter enables color images to be captured by transmitting red, green or blue light. Between the inner lens and the photodiode is the wiring layer. If too thick, it may prevent the light that has passed through the micro-lens, color filter and inner lens from reaching the photodiode or cause it to collect in a location other than the photodiode. By using copper (Cu) wiring, Sony was able to reduce the thickness of the wiring layer, allowing the light to be collected effectively in the photodiode.





Reducing Noise

However efficiently signals are generated, a good signal-to-noise ratio cannot be achieved if noise is introduced at this stage. If there are defects in the silicon from which the pixel is made, the resulting thermal excitation of the electrons will cause dark-current noise. Under certain conditions, even a single-electron noise will be visible in the image. For this reason, the reduction of dark-current noise is the most important priority when developing an image sensor. This is achieved by minimizing the occurrence of defects and contamination, and by shielding areas that are vulnerable to defects.

Row-Column-Row A/D Conversion for Enhanced Speed

The key to increased speed can be found in parallel signal processing. CMOS sensors have analogdigital (A/D) conversion circuits that convert analog pixel signals into digital signals (Figure 2). Speed is increased by arranging thousands of these circuits in a horizontal array and allowing them to operate simultaneously. The A/D conversion circuits used in Sony's CMOS sensors have important characteristics, including the reduced size of the analog circuits in which noise is created, and automatic noise cancellation. This circuit design enables noise reduction to be combined with





Figure 2: Column parallel A/D Conversion Circuit

Pixel signals are read as output from the transistors in the pixel. However, there is variation in the threshold voltages for the transistors in each of the millions of pixels. This variation can be eliminated by reading just the original pixel signal (VSIG), which is obtained by reading the difference between the initial value (reset level, VRST) of each transistor and the signal level corresponding to the incident light (VSIG+VRST) through correlated double sampling (CDS). Sony's CMOS sensors perform this CDS operation by means of digital signal processing.



Figure 3: A/D Converter Technique Timing Chart

The reset level (VRST) is detected during counter down-count (primary digital sampling).

- After detection of the reset level, the signal level (VSIG+VRST) is detected by up-counting from the state at which the counter value was saved (secondary digital sampling).
- ③ The net signal value (VSIG) is detected by subtracting the reset level(VRST) from the final count value(VSIG+VRST). This digital subtraction process can also be used to cancel out variation in the characteristics of comparators in each column, and in the way in which the ramp waves used for comparison are transferred. This allows rapid A/D conversion with minimal noise.

Future Challenges

Image sensors are used in video and digital still cameras. In the video camera market there has been an accelerating shift toward HD models, while in the digital still camera market pixel counts have continued to rise, and digital SLR cameras are becoming increasingly popular. There has also been a rapid increase in mobile phone camera resolution. Sony will continue to support the evolution of these applications by increasing the speed and pixel counts of its CCD and CMOS sensors. To achieve higher pixel counts, pixels must be made smaller. However, sensitivity is generally proportional to pixel area and will decline if pixel size is reduced. By combining its knowledge of the technology developed for CCDs, Sony has been able to compensate for the sensitivity loss caused by reductions in pixel size. The future goal is to combine higher speeds with higher resolutions while compensating for reductions in sensitivity resulting from reductions in pixel size. This will be achieved using device process technology, circuit technology and image processing technology.

Figure 4 shows a sequence of images captured using the CMOS Sensor "Exmor". Sony wants to create devices so that users can seamlessly capture high-resolution images without worrying about whether the camera is in video or still mode, and which enables them to easily record phenomena that previously required professional-use cameras equipped with specialized image sensors.

Sony has enhanced the read-out method used in its CMOS sensor to allow high-speed photography at over 300 frames per second.



Figure 4: A sequence of photographs showing a water balloon in mid-burst

Interviews with engineers

Vol.6 35mm Full-size CMOS Sensor **Awards**

In June 2006, a paper on Sony's High-Speed CMOS Sensor won the Walter Kosonocky Award. This award is presented bi-annually for papers published anywhere in the world concerning image sensors.

Copyright 2012 Sony Corporation